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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,445	FURUSHO, SHINJI	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/10/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/553445 has a total of 25 claims pending in the application, there are 7 independent claims and 18 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. ' 1.63**.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. ' 201.14(c)**, acknowledgment is made of applicant's claim for priority based on an application filed in Japanese Application JP 2003/111978 on April 16, 2003.

INFORMATION CONCERNING DRAWINGS

Drawings

The applicant's drawings submitted 10/17/2005 are acceptable for examination purposes.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

As required by **M.P.E.P. ' 609 (C)**, the applicant's submission of the Information Disclosure Statement, dated 7/10/2006, is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P. ' 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

CLAIM OBJECTIONS

Claim 35 is objected to because of the following informalities: 'resister group' is thought to mean 'register group' based on Paragraph 0303 in the specification. Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections – 35 USC '101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 45 is rejected under 35 U.S.C. 101 because it is directed to a program, which is software *per se*. Software does not appear to be statutory subject matter, and the examiner suggests amending the claim such that the program is embodied on a hardware medium.

Claim Rejections - 35 USC ' 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 33-34 and 43-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 33 and 43 recite the limitation "'the fifth global ordered set array" in and the last few words of each claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 35 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim states that an operating using the array is executed without accessing a memory, though one of ordinary skill in the art could say that a register group is a memory. The phrase has been construed to mean 'without accessing an external memory'.

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-34 and 36-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furusho '332 (EP 1,233,332) in view of Furusho '918 (EP 1,136,918)

Regarding Claim 26, Furusho '332 teaches an information processing system comprising: plural information processing units (Blocks 14-1 to 14-4 in Figure 1) each holding a local information block (such as the blocks in Figure 6) to express tabular data expressed as an array of records including an item and item values belonging to the item (where the items correspond to the entries in Figure 6 and the item values correspond to the values contained in these entries, such as 'Carter'); and

a packet transmission path to connect the plural information processing units (bus 26 in Figure 1, described in paragraph 0034); and

the information processing unit is characterized in that each of the information processing units includes: means for creating, based on the numbers to indicate the local order in the local information block (this local order is indicated by the 'subscripts' as described in paragraph 0052), numbers to indicate a unique global order in all the plural information processing units (all elements are ordered during the merge in step 710 in Figure 7, also see paragraph 0086, also see Column 2 Line 55 to Column 3 Line 21, where it is made clear that the information on the individual processor modules are first ordered before a global order [the global order indicated by virtual sequence numbers, Column 19 Lines 22-26] is decided); means for transmitting the value list to another information processing unit through the packet transmission path; means for receiving a value list from the another information processing unit through the packet transmission path (see beginning of paragraph 0063, where two elements

[corresponding to the value list] are transmitted to another processor, thus the processors are able to give and receive value lists); and means for giving, by referring to an item value in the value list from the another information processing unit, a global order in all the plural information processing units to the item value in the value list in the local information block (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"], also note that this global order is found by referring to item values from previous processors, see paragraphs 0058 and 0060).

However, Furusho '332 does not explicitly teach how the records are stored within the processors. Furusho '918 teaches storing information on a local information block, including a value list in which the item values are stored in order of item value numbers corresponding to item values belonging to a specific item (see Figure 7, where the item value 'age' numbers are stored in order, and the specific item is the 'age' category), and a pointer array in which pointer values to indicate the item value numbers are stored in order of numbers to indicate a unique local order corresponding to the records (where the table of pointers on Figure 7 are indexed to a unique local order [since the rows indicate the record number as in the last sentence of paragraph 0012], and they each contain a pointer to the item value [age]).

It would have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made to have stored the records of Furusho '332 as in Furusho '918, since storing the records this way helps to increase greatly the speed of searching for and tabulating large amounts of data (Paragraph 0009 in Furusho '918).

Regarding Claim 27, Furusho '332 teaches an information processing system comprising: plural memory modules each having a memory, an interface, and a control device (memory modules 14, which have memory for storing data as shown in Figure 4, an interface as shown Figure 3, and a controller corresponding to a processor as described in Paragraph 0051);

and a packet transmission path connecting interfaces of the adjacent memory modules (bus 26 in Figure 1, described in paragraph 0034),

and a global information block is formed of an aggregate of the information blocks held in the respective memories (see paragraph 0086, where the sequence of all elements are determined, and from this global array [corresponding to a global information block] can be determined in step 711 of Figure 7),

and memory of the memory modules holds an information block including a value list which is for expressing tabular data expressed as an array of records each including an item and an item value belonging to the item (where the items correspond to the entries in Figure 6 and the item values correspond to the values contained in these entries, such as 'Carter');

and the information processing system is characterized in that the control device of each of the memory modules includes: offset value storage means for holding an offset value to indicate that its own grasped information block, as a subset of the global information block, occupies which position in the pointer array (this offset is indicated by the 'subscripts' as described in paragraph 0052);

global ordered set array creation means for creating, based on the offset value, a

global ordered set array in the global information block (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"], also note that this global order is found based on the offset values [subscripts as defined in paragraph 0052] from previous processors, see paragraphs 0058 and 0060); packet transmission means for packeting its own value list of an item and transmitting it by using the transmission path between the adjacent memory modules (see beginning of paragraph 0063, where two elements [corresponding to the value list] are transmitted to another processor, thus the processors have packet transmission to transmit value lists);

packet reception means for receiving a packeted value list of another memory module by using the transmission path in parallel to packet transmission by the packet transmission means (see beginning of paragraph 0063, where two elements [corresponding to the value list] are transmitted to another processor, thus the processors have packet reception means to receive value lists); and

order judgment means for determining an order, in the global information block, of the item value in its own value list of the item by referring to the received respective value list and for storing the order, in the global information block, of the item value into a global value number array relating to the item (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"], also note that this global order is found by referring to item values [subscripts as defined in paragraph 0052] from previous processors, see paragraphs 0058 and 0060, thus the processors have order judgment means, and once this global order is found it is stored in the global information block as constructed in step 711 of Figure 7).

However, Furusho '332 does not explicitly teach how the records are stored within the memory modules. Furusho '918 teaches where memory of each of the memory modules contain item values which are stored in order of item value numbers corresponding to the item values belonging to a specific item (see Figure 7, where the item value 'age' numbers are stored in order, and the specific item is the 'age' category), and a pointer array in which pointer values to indicate the item value numbers are stored in a unique order of an ordered set array (the pointer array corresponding to the table of pointers on Figure 7 are indexed to a unique local order [since the rows indicate the record number as in the last sentence of paragraph 0012], and they each contain a pointer to the item value [age]).

It would have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made to have stored the records of Furusho '332 as in Furusho '918, since storing the records this way helps to increase greatly the speed of searching for and tabulating large amounts of data (Paragraph 0009 in Furusho '918).

Regarding Claim 28, Furusho '332 and Furusho '918 teach the information processing system according to claim 27, and Furusho '332 further teaches that the order judgment means is constructed to calculate the order in the global information block by adding a total sum of differences between the judged respective relative orders and the original order to the original order (note how the difference is calculated from the relative orders [virtual sequence number] and the original sequence number [the sequence at the time of sending of the element in step c], Column 6 Lines 22-26 and

step 3132-2 in Figure 31C, and the total sum of these numbers is subsequently calculated to find an order in the global information block as in step 3135 in Figure 31C).

Regarding Claim 29, Furusho '332 and Furusho '918 teach the information processing system according to claim 27, and Furusho '332 further teaches that the order judgment means compares the transmitted packet and the received packet and deletes a duplicate value (Column 32 Lines 21-49, where the element corresponds to the value).

Regarding Claim 30, Furusho '332 and Furusho '918 teach the information processing system according to claim 27, and the storage table of Furusho '918 further includes:

flag array setup means for creating, with respect to an item to be retrieved, a flag array with a same size as the value list of the item and for giving a specific value to an inside of the flag array corresponding to an item value coincident with a retrieval condition (see Figure 7, where the value control table is the flag array, since this table is the same size as the value list [one row for each value, or age] and each row contains a specific value [the age] which can be retrieved as in the process of Column 6 Lines 17-23, thus flag array setup means to create such a table is present);

retrieval condition judgment means for judging whether a record corresponding to a value in the ordered set array is coincident with the retrieval condition by specifying, with respect to the item to be retrieved, a value in the pointer array corresponding to a position indicated by the ordered set array (the position corresponding to the entry number of the pointer table in Figure 7) and then by specifying a value in the flag array

corresponding to a position indicated by the value in the pointer array (the pointer at the corresponding record specifies the value in the value table of Figure 7, also see Column 6 Lines 8-23, thus such judgment means are present);

and Furusho '332 teaches a local retrieval means for storing a value of an ordered set coincident with the retrieval condition (see Figure 6, where the set is ordered with the retrieval condition corresponding to the last name) and a value of a corresponding global ordered set into a second ordered set array and a second global ordered set array (where the re-ordered set of Figure 6 corresponds to the second global ordered set array),

wherein the packet transmission means uses the transmission path, packets the second global ordered set array and transmits it, the packet reception means uses the transmission path and receives a packeted second global ordered set array of another memory module (see beginning of paragraph 0063, where two elements [corresponding to the global ordered list] are transmitted to another processor, thus packet transmission and reception means are present),

there is further included second order judgment means for determining an order, in the global information block, of a value in its own global ordered set array by referring to the received respective second global ordered set array and for storing the order in the global information block into a third global ordered set array (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"], also note that this global order is found by referring to item values from the second global ordered set [subscripts as defined in paragraph 0052] from previous processors, see

paragraphs 0058 and 0060, thus second order judgment means are present, and once this global order is found it is stored in a third global ordered set array as constructed in step 711 of Figure 7 and explained in paragraph 0086), and

an order of a record coincident with the retrieval condition is decided by a value of the third global ordered set array (a new ordered array is generated as in Column 26 Liens 23-28).

Regarding Claim 31, Furusho '332 and Furusho '918 teach the information processing system according to claim 27, and Furusho '918 further teaches that the control device contains count-up means for creating, with respect to items to be tabulated, a logical coordinate array with a size obtained by multiplying sizes of value lists of the items (such a logical coordinate array corresponding to the Table of Figure 26, also see process for creating this table in Figure 20, note how the number of entries [size] is calculated by multiplying the number of item values [3 for gender and 5 for occupation, resulting in 15 values]) and for acquiring the number of records for each set of item values of each item by counting up values of the logical coordinate array indicated by values in the ordered set array and corresponding to the sets of the values in the pointer arrays of the items to be tabulated (as show in steps 204, 206, 208, and 210 in Figure 22), and

the packet transmission means uses the transmission path, and packets and transmits the logical coordinate array in which count-up has been performed by the count-up means (see beginning of paragraph 0063 in Furusho '332, where two elements [containing the logical coordinate array of Furusho '918] are transmitted to

another processor, thus packet transmission and reception means are used and the array transmitted), the number of records for each set of item values of each global item is stored in the logical coordinate array by sequentially executing, in each of the memory modules, the count-up of the same logical coordinate array and the transmission using the transmission path (Paragraph 0086 in Furusho '332, where a global order is given ["sequence number of all elements are determined"], and thus the counts are made again at the time of re-tabulation of the global sequence, note Column 5 Lines 43-49 in Furusho '918, particular where the count-tables become 'usable at the time of tabulating'), and in each of the memory modules, the packet reception means and the packet transmission means sequentially execute reception and storage of the logical coordinate array in which the count-up has been ended (since the tabulation is updated at the time of tabulating as in Column 5 Lines 43-39 in Furusho '918, the reception means and packet transmission means sequentially execute the logical coordinate array storage, i.e., the count is updated as the next array element comes in), and the transmission using the transmission path (the transmission path [bus] 26 of Figure is used for transmission as described in paragraph 0036 of Furusho '332).

Regarding Claim 32, Furusho '332 and Furusho '918 teaches all limitations of Claim 31 as described above, wherein count-up means creates, with respect to items to be tabulated, a multi-dimensional count-up array with a size obtained by multiplying sizes of value lists of the items (such a logical coordinate array corresponding to the Table of Figure 26, also see process for creating this table in Figure 20, note how the number of entries [size] is calculated by multiplying the number of item values [3 for

gender and 5 for occupation, resulting in 15 values], also note how the array is clearly multi-dimensional as described in step 204), acquires the number of records for each set of item values of each item by counting up values in the count-up array indicated by values in the ordered set array and corresponding to the set of values in the pointer arrays of the items to be tabulated (as explained in steps 204, 206, 208, and 210 of Furusho '918), and arranges, in the logical coordinate array in which mapping to position in the count-up array is made, a value in the count-up array in accordance with the mapping (the entry corresponding to the entries in the array of Figure 26 of Furusho '918).

Regarding Claim 33, Furusho '332 and Furusho '918 teaches all limitations of claim 27 as described above, and Furusho '918 further teaches the control device of each of the memory modules includes:

existence number array creation means for creating, with respect to an item to be sorted, an existence number array with a same size as a value list of the item and for arranging the number of values (the logical count-up array corresponding to the 'count' category array of Figure 7, which is the same size as the value array on the other side of the table), to specify respective item values in the value list, of the ordered set array (each entry in the array is a count of the number of values in the ordered set array, thus, since such an array is created, existence number array creation means are present) ;

accumulated number array creation means for accumulating values in the existence number array, calculating an accumulated number to indicate a head position of a record having a corresponding item value at a time when the sort is performed in

the memory module (the table of Figure 7 contains a start [head] position of the records having the corresponding item value at that particular row position, and since this array is created at the time of tabulating as described at the end of paragraph 0017, the item value of the record corresponds to when the sort was performed), and arranging the accumulated number in an accumulated number array (the accumulated number is clearly arranged in the array as shown in Figure 7); and Furusho '332 further teaches

local sort means for creating a second global value number array, a fourth global ordered set array and a third ordered set array (each memory unit 14 has a local sort means that re-sorts the data [as shown in Figure 6] and forms second, third, and fourth set arrays which contain global sequence numbers, see paragraphs 0054 and 0055 in Furusho '332), arranging a global value number corresponding to the item value at a position indicated by the accumulated number in the second global value number array based on the accumulated number in the accumulated number array corresponding to an item value indicated by a value of the ordered set array (Paragraph 0086, where a global order is given based on an item value ["sequence number of all elements are determined"], also note that this global order is found by referring to item values from the second global ordered set from previous processors as shown in Paragraphs 0058 and 0060, and since a sequence is given according to these item values as described in Paragraph 0060, and the set array stores the beginning of the sequences of the item values, that this order is found by referring to the position of the accumulated number), and arranging a value of the ordered set array and a value of the corresponding global ordered set array at a position indicated by the accumulated number in the third ordered

set array and the fourth global ordered set array (note how the process applied to the first and second arrays is done in a similar fashion to the third and fourth arrays, see Paragraph 0069 in Furusho '334);

wherein the packet transmission means uses the transmission path, and packets and transmits at least the second global value number array, and the packet reception means uses the transmission path in parallel and receives a packeted second global value array of another memory module (see beginning of paragraph 0063 in Furusho '332, where two elements [containing the array of Furusho '918] are transmitted to another processor, thus packet transmission and reception means are used and the array transmitted),

there is further included third order judgment means for storing an order, in the global information block, of a value in its own second global value number array into the fifth global ordered set array (a new fifth order set array is created as in Paragraph 0086, and this is of course based on the value of the ordered global information blocks because of the processing done in paragraphs 0058 and 0060), and

an order of the sorted record is decided by the value of the fifth global ordered set array (since the fifth global order is stored as in paragraph 0086, the order of the sorted records is decided by it).

Regarding Claim 34, Furusho '918 and Furusho '332 teach all limitations of Claim 33 as described above. Furusho '332 furthers teaches that the packet transmission means packets and transmits the second global value number array and the fourth global ordered set array by pairing a value of the second global value number

array and a value of the fourth global ordered set array (the transmission process of Furusho '332 teaches pairing the third and fourth as in paragraph 0069, though the beginning of paragraph 0056 implies that there could be other pairs such as the second and fourth global ordered set arrays), the packet reception means receives the packeted second global value number array and fourth global ordered set array of another memory module (packet reception means receive these ordered set arrays in a hierarchical manner as in Column 25 Line 58 to Column 26 Line 9, thus as one moves up the hierarchy these memory modules receive second and fourth global value numbers), and

the third order judgment means judges an order by comparing, when a value of its own second global value number array and a value of the second global number array of another memory module are equal, values of the fourth global ordered set arrays forming a pair of the respective values (the judgment means orders all elements from the ordered set arrays as in Paragraph 0086, and does so even when some elements from the global number array modules are equal as in Column 29 Lines 17-24).

Claim 36 is the method equivalent of Claim 26 and is rejected under similar rationale.

Claim 37 is the method equivalent of Claim 27 and is rejected under similar rationale.

Claim 38 is the method equivalent of Claim 28 and is rejected under similar rationale.

Claim 39 is the method equivalent of Claim 29 and is rejected under similar rationale.

Claim 40 is the method equivalent of Claim 30 and is rejected under similar rationale.

Claim 41 is the method equivalent of Claim 31 and is rejected under similar rationale.

Claim 42 is the method equivalent of Claim 32 and is rejected under similar rationale.

Claim 43 is the method equivalent of Claim 33 and is rejected under similar rationale.

Claim 44 is the method equivalent of Claim 34 and is rejected under similar rationale.

Claim 45 is the program equivalent of Claim 26 and is rejected under similar rationale.

Regarding Claim 46, Furusho '332 teaches an information processing system comprising: plural information processing units each including a memory and a control device (memory modules 14, which have memory for storing data as shown in Figure 4, an interface as shown Figure 3, and a controller corresponding to a processor as described in Paragraph 0051), wherein the memory of each of the information processing units holds tabular data expressed as an array of records each including an item and an item value belonging to the item (where the items correspond to the entries in Figure 6 and the item values correspond to the values contained in these entries,

such as 'Carter'),

global tabular data is formed of an aggregate of tabular data held by respective memory modules (as in paragraph 0086), and the information processing system is characterized in that each of the information processing units includes:

a local ordered set array containing values indicating local orders of the respective records in the information processing unit (this local order is indicated by the 'subscripts' as described in paragraph 0052);

a global ordered set array containing values indicating orders of the respective records in the global tabular data (all elements are ordered during the merge in step 710 in Figure 7, also Figure 12, where the global sequence is shown to be formed).

However, Furusho '332 does not explicitly teach record extraction means. Furusho '918 teaches

record extraction means for specifying a value in the global ordered set array in accordance with an instruction to specify an order received by the control device, for specifying a value in the local ordered set array (see the extraction of paragraph 0012, where the record number is the value in the global ordered set array and the extraction must be done in accordance with an instruction), a position of said value in the local ordered set array being consistent with that of the value in the global ordered set array (the position being the certain record number as specified in paragraph 0012), and for extracting the record indicated by the value in the local ordered set array (the values corresponding to this record are extracted, note how all data field values can be extracted as in the last sentence of paragraph 0012).

It would have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made to have stored the records of Furusho '332 as in Furusho '918, since storing the records this way helps to increase greatly the speed of searching for and tabulating large amounts of data (Paragraph 0009 in Furusho '918).

Regarding Claim 47, Furusho '332 and Furusho '918 teach all limitations of Claim 46 as described above. Further, Furusho '332 teaches the information processing unit being adopted such that,

in order to reflect a sort order in the information processing unit, in case that the values in the local ordered set array are exchanged (in the case where the data is exchanged among the processing units as in Column 22 Lines 11-16) ,

in the global ordered set array, the value indicating the order is rearranged to indicate a sort order, in the global tabular data, of the record indicated by the value in the another ordered set array (note the global sequence values indicating the order is rearranged because of this exchange in Figures 16-19).

Regarding Claim 48, Furusho '332 and Furusho '918 teach all limitations of Claim 46 as described above. Further, Furusho '332 teaches the information processing unit to be characterized in that the information processing unit rearranges the value indicating the order to indicate the sort order, in the global ordered set array, of the record sorted in the information processing unit (note the global sequence values indicating the order is rearranged because of this exchange in Figures 16-19).

Regarding Claim 49, Furusho '332 and Furusho '918 teach all limitations of

Claim 46 as described above, and Furusho '918 further teaches characterized in that the information processing unit rearranges the value indicating the order to indicate the so (note the global sequence values indicating the order is rearranged because of this exchange in Figures 16-19) that a memory of each of the information processing units holds an information block (the memory information block corresponding to the blocks as in Figure 10 in Furusho '332) including a value list which is for expressing tabular data expressed as an array of records each including an item and an item value belonging to the item and in which the item values are stored in order of item value numbers corresponding to item values belonging to a specific item (see Figure 7, where the item value 'age' numbers are stored in order, and the specific item is the 'age' category), and a pointer array in which pointer values to indicate the item value numbers are stored in a unique order of an ordered set array (where the table of pointers on Figure 7 are indexed to a unique local order [since the rows indicate the record number as in the last sentence of paragraph 0012], and they each contain a pointer to the item value [age]), and

a global information block is formed of an aggregate of the information blocks held in the respective memories (as in Paragraph 0086 in Furusho '332).

Regarding Claim 50, Furusho '332 and Furusho '918 teach an information processing system comprising

plural information units each including a memory and a control device (memory modules 14, which have memory for storing data as shown in Figure 4 and a controller corresponding to a processor as described in Paragraph 0051),

a global information block is formed of an aggregate of the information blocks held in the respective memories (Paragraph 0086, where a global order corresponding to a global information block is given ["sequence number of all elements are determined"], also note that this global order is found by referring to item values from previous processors, see paragraphs 0058 and 0060), and the information processing system is characterized in that the information processing unit includes:

a global value number array to contain a value indicating an order of an item value in a global information block (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"]); and Furusho '918 teaches a table wherein:

a memory of each of the memory modules holds an information block including a value list which is for expressing tabular data (the information block as shown in Figure 6) expressed as an array of records each including an item and an item value (where the items correspond to the entries in Figure 6 and the item values correspond to the values contained in these entries, such as 'Carter') belonging to the item and in which item values are stored in order of item value numbers corresponding to the item values belonging to a specific item (see Figure 7, where the item value 'age' numbers are stored in order, and the specific item is the 'age' category), and a pointer array in which pointer values to indicate the item value numbers are stored in a unique order of an ordered set array (where the table of pointers on Figure 7 are indexed to a unique local order [since the rows indicate the record number as in the last sentence of paragraph 0012], and they each contain a pointer to the item value [age]), and

item value extraction means for specifying a value in the global value number array in accordance with an instruction to specify an order received by the control device and for extracting an item value in the value list indicated by the value (see the extraction of paragraph 0012, where the record number is the value in the global ordered set array and the extraction must be done in accordance with an instruction).

It would have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made to have stored the records of Furusho '332 as in Furusho '918, since storing the records this way helps to increase greatly the speed of searching for and tabulating large amounts of data (Paragraph 0009 in Furusho '918).

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furusho '332 (EP 1,233,332) and Furusho '918 (EP 1,136,918) in further view of Yip (US 2002/0027516).

Regarding Claim 35, Furusho '918 and Furusho '332 teach all limitations of Claim 27 as described above. However, neither reference explicitly teaches the memory module including a register group for use as the array. Yip teaches using registers to form an array (middle of paragraph 0058), which would mean an external memory would not have to be accessed when accessing an array, since the array is in the register. It would have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made to have included the registers of Yu in the memory modules of Furusho '332 because registers are much

faster than external memory. Thus, by combining the devices, additional benefits are obtained.

CLOSING COMMENTS

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

SUBJECT MATTER CONSIDERED ALLOWABLE

CLAIMS NO LONGER IN THE APPLICATION

Claims 1-25 were cancelled by the amendment dated 10/17/2005.

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 26-50 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

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Patent Examiner
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April 15, 2008

/Sanjiv Shah/
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